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Customer No. 22,852
Attorney Docket No. 04329.2762

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Yasuyuki NOZUYAMA

Serial No.: Not Yet Assigned

Filed: March 7, 2002

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND TEST METHOD THEREOF

Group Art Unit: Not assigned

Examiner: Not assigned

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicant brings to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicant respectfully requests that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicant determines

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that the cited documents do not constitute "prior art" under United States law, applicant reserves the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: March 7, 2002

By: _____
Richard V. Burgujian
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Enclosures
RVB/FPD/dvz

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OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.2762	Serial No.	
Applicant	Yasuyuki NOZUYAMA		
Filing Date	March 7, 2002	Group:	Not assigned

J1050 U.S. PTO 10/091552 03/07/02

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		5,184,067	2/2/93	Nozuyama			
		6,223,312 B1	4/24/01	Nozuyama			
		4,377,757	3/22/83	Könemann et al.			
		5,677,916	10/14/97	Nozuyama			
		5,867,409	2/2/99	Nozuyama			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Yasuyuki NOZUYAMA, "Semiconductor Integrated Circuit Including A Test Facilitation Circuit For Functional Blocks Intellectual Properties And Automatic Insertion Method Of The Same Test Facilitation Circuit" Serial No. 09/960,414 filed September 24, 2001.

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce